REMARKS

Entry of this Amendment is proposed because it does not raise any new issues requiring further search, narrows the issues on appeal and does not require further search by the Examiner.

Claims 15-17 and 22 are all the claims presently pending in the application.

Claim 16 is rewritten in independent form and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant gratefully acknowledges that claim 17 would be allowable if rewritten in independent form. However, for the following reasons, Applicant respectfully submits that all of the claims (i.e., claims 15-17 and 22) are allowable.

With respect to the prior art rejection, claims 15, 16, and 22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Takano et al. (U.S. Patent No. 5,790,874, hereinafter "Takano").

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of reducing power in a portable microprocessor.

In an illustrative, non-limiting embodiment of the invention as defined by independent claim 15, a method of reducing power in a portable microprocessor includes obtaining an opcode group and obtaining a control signal therefrom, determining whether the control signal is active,

if the control signal is determined to be active, setting the control signal to active, running a test case for the opcode group to determine whether the opcode passes, and if the opcode group passes, marking the control signal.

In another exemplary embodiment of the invention, as defined by independent claim 16, the method further includes determining whether any other control signals exist for the opcode group, when no more control signal exists, obtaining a next opcode group and testing and determining whether control signals of the next opcode should be marked, and when no more opcode groups exist, setting all marked control signals to active and executing a regression analysis thereon.

In another exemplary embodiment of the invention, as defined by independent claim 22, a signal-bearing medium tangibly embodying a program of machine-readable instructions executed by an apparatus to perform a method of reducing power in a portable microprocessor includes obtaining an opcode group and obtaining a control signal therefrom, determining whether the control signal is active, if the control signal is determined to be active, setting the control signal to active, running a test case for the opcode group to determine whether the opcode passes, and if the opcode group passes, marking the control signal.

The claimed invention, which may be termed an "Auto_Don't _Care (ADC)" method, automates the finding of control bits which need not toggle, and frees the designer from having to do a manual search for such bits (e.g., see specification at page 16, lines 13-16).

In the claimed invention, the opcode will maintain the previous control signals to a previous state, and will change only the control signals required for the current cycle's operation (e.g., see specification at page 15, lines 18-20). That is, the claimed invention determines what

control signals could be left at the previous state and what control signals could be changed to new values (e.g., see specification at page 15, lines 21-24).

Thus, the claimed invention provides significant time savings, thereby reducing the time to debug from months (e.g., by human related art methods) to hours/days (e.g., by the claimed method) (e.g., see specification at page 16, lines 16-18). The claimed invention also provides for automated debugging (e.g., see specification at page 16, line 18).

II. THE PRIOR ART REJECTION

Claims 15, 16, and 22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Takano et al. (U.S. Patent No. 5,790,874, hereinafter "Takano").

For the Examiner's convenience, Applicants' remarks as submitted in the Amendment filed on February 4, 2004, are incorporated herein by reference.

A. Independent Claim 15:

In the Response to Arguments, the Examiner alleges that Takano (e.g., see Takano at column 11, line 62-67) discloses obtaining an opcode group and obtaining a control signal therefrom (see Office Action at page 3, numbered paragraph 5).

Particularly, the Examiner compares the instructions of Takano to the claimed opcode group and the optimized instruction sequences stored in the variable MinHdSequence to the claimed control signal (see Office Action at page 3, numbered paragraph 5).

Moreover, the Examiner alleges that Takano discloses the claimed "determining whether said control signal is active" and "setting the control signal to active" by storing the last instruction stored in the MinHdSequence into the LastCom variable, which allegedly is

representative of the instructions sequences that were optimized (see Office Action at page 3, numbered paragraph 6).

Applicants respectfully disagree with the Examiner's position for several reasons.

In contrast to Takano, Applicants respectfully reiterate that the claimed invention provides a method, such that unnecessary toggling between bits of control signals is minimized.

For example, an opcode will correspond to a particular state for the control signals of the microprocessor. The present invention minimizes toggling between a control signal of an opcode by looking to the previous state of the control signal. When the control signal matches that of the previous state, there in no need to set the control signal to a value, i.e., the control signal is marked.

That is, as mentioned above, in the claimed invention, the opcode will maintain the previous control signals to a previous state, and will change only the control signals required for the current cycle's operation (e.g., see specification at page 15, lines 18-20). Hence, the claimed invention determines what control signals could be left at the previous state and what control signals could be changed to new values (e.g., see specification at page 15, lines 21-24).

For example, independent claim 15 recites "a method of reducing power in a portable microprocessor includes obtaining an opcode group and obtaining a control signal therefrom, determining whether the control signal is active, if the control signal is determined to be active, setting the control signal to active, running a test case for the opcode group to determine whether the opcode passes, and if the opcode group passes, marking the control signal" (emphasis added).

In other words, the claimed method automates the finding of control bits which need not toggle and frees the designer from having to do a manual search for such bits (e.g., see

specification at page 16, lines 13-16). As such, the claimed invention provides significant time savings, thereby reducing the time to debug and also providing for automated debugging.

On the other hand, Takano merely discloses an instruction sequence optimization method.

Particularly, in Takano, sequences of instructions are modified to reduce the Hamming distances between bit sequences appearing on the instruction bus without influence on the dependent relation (e.g., see Takano at column 9, lines 41-44; see also Figure 2, step 203).

In other words, Takano discloses that low power consumption caused on the instruction bus can be achieved by the modification of the instructions sequences (e.g., see Takano at column 9, lines 44-46). Takano seeks to reduce power consumption on an instruction bus by optimizing a sequence of instructions, such that differences in bit sequences (and the toggle between states necessitated by these differences) between successive instructions are minimized.

Applicants note that, while Takano discusses "do not care" bits, Takano merely discloses that there are some cases where "do not care" bits are included in the instructions format (e.g., see Takano at column 13, lines 48-52). Takano discloses that "[t]here are some cases wherein Hamming distances between adjacent instructions can be reduced by modifying such bit values suitably" (e.g., see Takano at column 13, lines 54-57), which clearly is a different method than the claimed invention which determines which control signals can be left at a previous state and which can be changed to new values.

Indeed, although Takano mentions "do not care" bits, Takano clearly is concerned with reducing Hamming distances as a method of reducing power consumption, and not with determining what control signals could be left at the previous state and what control signals could be changed to new values as a method of reducing power consumption (e.g., determining

whether the control signal is active, if the control signal is determined to be active, setting the control signal to active, running a test case for the opcode group to determine whether the opcode passes, and if the opcode group passes, marking the control signal), according to the claimed invention.

In contrast to Takano, Applicants respectfully reiterate that the claimed invention provides a method in which unnecessary toggling between bits of control signals can be minimized, not an instruction sequence optimization method, as set forth in Takano.

Thus, for at least the foregoing reasons, Applicants respectfully submit that Takano neither discloses nor suggests all of the features of independent claim 15, and therefore, respectfully requests that the Examiner withdraw the rejection of claim 15 and permit claim 15 to pass to allowance.

B. Independent Claim 16:

Claim 16 is rewritten in independent form.

In another exemplary embodiment of the invention, as defined by independent claim 16, the method further includes "when no more opcode groups exist, setting all marked control signals to active and executing a regression analysis thereon" (emphasis added).

Applicants respectfully submit that Takano neither discloses nor suggests at least this feature of the claimed invention defined by independent claim 16.

Indeed, the Examiner the Examiner has not identified any specific disclosure, teaching, or suggestion in Takano for this feature, but instead, generally refers to Takano at column 10, line 36 to column 11, line 9 (see Office Action at page 3, lines 1-3).

Applicants respectfully request that the Examiner consider each of the features of independent claim 16 and specifically identify the support, in the Takano reference, for each of the claimed features that the Examiner is relying on to establish the alleged anticipation of claim 16.

Nevertheless, Applicants respectfully submit that Takano neither discloses nor suggests at least these features, as recited in independent claim 16.

Therefore, Applicants respectfully request that the Examiner withdraw this rejection and permit independent claim 16 to pass to allowance.

C. Independent Claim 22:

With respect to independent claim 22, Applicant respectfully submits that claim 22 is patentable over Takano for somewhat similar reasons as those set forth above with respect to independent claim 15, and therefore, respectfully requests that the Examiner withdraw this rejection and permit claim 22 to pass to allowance.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 15-17 and 22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: June 28, 2004

John J. Dresch, Esq.
Registration No. 46,672

Sean M. McGinn
Registration No. 34,386

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 the enclosed Amendment under 37 C.F.R. § 1.116 to Examiner Yolanda L. Wilson on June 28, 2004.

John J. Dresch, Esq.
Registration No. 46,672
Sean M. McGinn, Esq.
Registration No. 34,386